Claims

What is claimed is:

[0047] 1. In a system comprising a processor configured to execute program code instructions stored in a program store, a pre-stored vector interrupt handling system, comprising:

an interrupt vector store comprising a plurality of interrupt vectors;

an interrupt control device connected to a plurality of interrupt request signals, said interrupt control device outputting an interrupt request signal to the processor; and

a selector, responsive to the processor's cycle type signal, for selecting between a program code instruction from the program store and an interrupt vector from said interrupt vector store to be loaded into an execution unit of the processor.

[0048] 2. The pre-stored vector interrupt handling system of claim 1, wherein the interrupt control device includes a prioritizer for prioritizing the plurality of interrupt request signals.

[0049] 3. The pre-stored vector interrupt handling system of claim 2, wherein the prioritizer asserts an interrupt identifier signal to the interrupt vector store for identifying which interrupt vector to load into said execution unit.

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[0050] 4. The pre-stored vector interrupt handling system of claim 1, wherein the interrupt control device comprises a means for masking the plurality of interrupt request signals.

[0051] 5. The pre-stored vector interrupt handling system of claim 4, wherein the masking means comprises a register for masking the plurality of interrupt request lines.

[0052] 6. The pre-stored vector interrupt handling system of claim 1, wherein the interrupt vector store is pre-programmed with interrupt vectors, each of said interrupt vectors being a branch instruction that jumps to an interrupt service routine in the program store.

[0053] 7. The pre-stored vector interrupt handling system of claim 1, wherein the interrupt vector store is implemented in read-only memory (ROM).

[0054] 8. The pre-stored vector interrupt handling system of claim 1, wherein the interrupt sources include one or more of data input devices, data output devices, embedded hardware devices, and data storage devices.

[0055] 9. The pre-stored vector interrupt handling system of claim 1, wherein the pre-stored vector interrupt handling system is incorporated in a computer system.

[0056] 10. The pre-stored vector interrupt handling system of claim 1, wherein the pre-stored vector interrupt handling system is incorporated in a microcontroller.

[0057] 11. The pre-stored vector interrupt handling system of claim 1, wherein the processor is a microprocessor.

[0058] 12. The pre-stored vector interrupt handling system of claim 11, wherein the microprocessor includes a cache.

[0059] 13. The pre-stored vector interrupt handling system of claim 12, wherein the microprocessor includes a means for pre-fetching instructions.

[0060] 14. The pre-stored vector interrupt handling system of claim 1, wherein the pre-stored vector interrupt handling system is included in a wireless communication device.

[0061] 15. The pre-stored vector interrupt handling system of claim 1 further comprising a multiplexer for selecting between an initialization mode and an interrupt mode.

[0062] 16. The pre-stored vector interrupt handling system of claim 1, wherein the selector is connected to a cycle type output signal from the processor.

[0063] 17. The pre-stored vector interrupt handling system of claim 16 wherein the selector asserts a chip select control signal to the interrupt vector store and de-asserts a chip select control signal to the program store if the cycle type output signal from the processor is an interrupt cycle, and de-asserts said control signal to the interrupt vector store and asserts said chip select signal to the program store if the cycle type output signal from the processor is a non-interrupt instruction cycle.

[0064] 18. The pre-stored vector interrupt handling system of claim 17, wherein the selector is connected to a read/write output signal from the processor, which read/write output signal is used by the selector to place the interrupt vector store into a read mode if the cycle type output signal from the processor is an interrupt cycle.

[0065] 19. The pre-stored vector interrupt handling system of claim 1, wherein the processor is a digital signal processor (DSP).

[0066] 20. In a system comprising a processor, a method for pre-stored vector interrupt handling, comprising the steps of:

intercepting a processor's normal instruction fetch bus cycle;

generating an interrupt identifier signal to the interrupt vector store; and

delivering a pre-stored interrupt vector directly to the execution unit of the processor, said pre-stored interrupt vector dependent upon said interrupt identifier signal.

[0067] 21. The method of claim 20 further comprising the step of initializing the interrupt vector store.

[0068] 22. The method of claim 21, wherein the step of initializing the vector store further comprises the step of pre-storing the interrupt vector store with a plurality of interrupt vectors.

[0069] 23. The method of claim 20, wherein the step of intercepting the processor's normal instruction fetch bus cycle further comprises the step of ensuring that the interrupt vector store has exclusive control of the data bus by asserting a chip select control signal to the interrupt vector store and deasserting a chip select control signal to the program store.

[0070] 24. A system for handling interrupts in a processor-controlled device, said processor-controlled device comprising a processor executing a software program stored as a set of program instructions, the system comprising:

an interrupt vector store;

an interrupt controller connected to a plurality of interrupt request signals, said interrupt controller outputting a master interrupt signal; and

a selector in a controlling arrangement with said interrupt vector store and with a memory storing program instructions being executed by the processor, said selector causing the processor to receive the next program instruction when the master interrupt

signal is not asserted, and to receive an interrupt vector (branch instruction op-code and address) from the interrupt vector store when the master interrupt signal is asserted.

[0071] 25. The system of claim 24, wherein said interrupt vector is provided directly to an execution unit of the processor.

[0072] 26. The system of claim 24, wherein said interrupt vector store is dynamically loaded with one or more interrupt vectors when the processor is running.

[0073] 27. The system of claim 24, wherein said interrupt vector store is statically pre-loaded with one or more interrupt vectors.

[0074] 28. The system of claim 24, wherein said processor is connected to a system bus, and wherein said selector causes the processor to receive the next program instruction by asserting a first select signal connected to said memory storing said program instructions when the master interrupt signal is not asserted, and causes the processor to receive said interrupt vector from the interrupt vector store by asserting a second select signal connected to said interrupt vector store when the master interrupt signal is asserted.

[0075] 29. The system of claim 24, wherein said interrupt vector store comprises a plurality of interrupt vectors, each interrupt vector corresponding to a different interrupt request signal.